REMARKS

The Office Action dated February 17, 2004, has been received and carefully considered. In this response, the specification has been amended. Entry of the amendments to the specification is respectfully requested. Reconsideration of the outstanding objections/rejections in the present application is also respectfully requested based on the following remarks.

I. THE OBJECTION TO THE DRAWINGS

On page 2 of the Office Action, the drawings were objected to under 37 CFR §1.84(p)(5) as not including references signs 404, 405, 504, 505, 604, 605, 704 and 705 mentioned in the description. The specification has been amended to overcome this objection. No new matter is entered.

In view of the foregoing, it is respectfully requested that the aforementioned objection to the drawings be withdrawn.

II. THE ANTICIPATION REJECTION OF CLAIMS 1-14 and 16-39

On page 3 of the Office Action, claims 1, 2, 5, 6, 9, 17-21, 23 and 33-39 were rejected under 35 U.S.C. § 102(b) as being anticipated by Coyle et al. (U.S. Patent No. 5,003,463). On page 4 of the Office Action, claims 1-14 and 17-39 were rejected under 35 U.S.C. § 102(e) as being anticipated by Garleep et al.

(U.S. Patent No. 6,687,780 B1). On page 6 of the Office Action, claims 10-16 and 24-32 were rejected under 35 U.S.C. § 102(e) as being anticipated by Borkar et al. (U.S. Patent No. 5,604,450). On page 8 of the Office Action, claims 10-16 and 24-32 were rejected under 35 U.S.C. § 102(e) as being anticipated by Ishibashi et al. (U.S. Patent No. 5,872,471). These rejections are hereby respectfully traversed.

Under 35 U.S.C. § 102, the Patent Office bears the burden of presenting at least a prima facie case of anticipation. In re Sun, 31 USPQ2d 1451, 1453 (Fed. Cir. 1993) (unpublished). Anticipation requires that a prior art reference disclose, either expressly or under the principles of inherency, each and every element of the claimed invention. Id. "In addition, the prior art reference must be enabling." Akzo N.V. v. U.S. International Trade Commission, 808 F.2d 1471, 1479, 1 USPQ2d 1241, 1245 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987). That is, the prior art reference must sufficiently describe the claimed invention so as to have placed the public in possession of it. In re Donohue, 766 F.2d 531, 533, 226 USPQ 619, 621 (Fed. Cir. 1985). "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his own knowledge to make the claimed invention." Id.

A. COYLE ET AL. REFERENCE

With respect to the Coyle et al. reference, the Office Action asserts that Coyle et al. teach the present invention as claimed. However, the Office Action fails to explain how Coyle et al. teach, or even suggest, "simultaneously transmitting a first portion of the first set of data from the first device to the second device over the common bus and transmitting a second portion of the first set of the data from the second device to the first device over the common bus," as recited in claim 1. Similar limitations are prevalent in independent claims 6, 17, 33 and 39.

The Office Action specifically asserts that Coyle et al. disclose a first device (18/20 and SBI 0 or MCU 22) operably coupled to a bus (SB 12), a second device (IOP 1 or MEM 0) operably coupled to the bus (SB 12), the first device (18/20 and SBI 0 or MCU 22) transmitting a first portion of a first set of data to the second device (IOP 1 or MEM 0) and the second device (IOP 1 or MEM 0) transmitting a second portion of the first set of data to the first device (18/20 and SBI 0 or MCU 22) simultaneously during a first exchange slot position.

The Office Action fails to mention how data is transmitted from a first device to a second device and second data is

transmitted from the second device to the first device, ***simultaneously over a common bus***. This claimed feature is clearly not supported structurally by Coyle et al. nor is it supported by the description provided by Coyle et al.. On page 12, the Office Action alleges that the IOP 1 or MEM 0 are operably coupled to the non-interlocked bus SB 12 and transmit sets of data over the bus SB 12 via I/O bus 42 or MEM bus 24. However, there is no support in Coyle et al. of any simultaneously transmission of data from a first device to a second device over a common bus. Rather, without any basis, the Office Action asserts that "common bus SB 12 does not prevent operation (data transmission of one device from interfering with another." However, a proper rejection under 102 requires more than just an assertion that a reference does not prevent a certain claimed operation. Instead, a valid disclosure of each and every claim limitation must be shown in a single reference.

The claims recite simultaneously transmitting data "over the common bus." The Office Action, however, makes no mention of how Coyle et al. teach simultaneous transmission of data over a common bus. In fact, the Office Action completely fails to address this feature.

Further, the structure of Coyle et al. relied upon by the Office Action fails to support the allegations made by the

Office Action. The first device (18/20 and SBI 0 or MCU 22) and second device (IOP 1 or MEM 0) do not transmit data simultaneously through system bus SB 12. Rather, second device IOP 1 and second device MEM 0 transmit data through IO Bus 42 and MEM BUS 24, respectively. First device 18/20 transmits data through common bus SB 12. First device SBI 0 transmits data with second device IOP 1 through IO BUS 42. First device MCU 22 transmits data with second device MEM 0 through MEM Bus 24. As supported by Coyle et al., SBI 34 communicates with the IOP's 44-50 through the IO Bus 42 and with the other system elements (18, MCU 22) through the System Bus 12 (column 8, lines 23-26). Thus, as supported by the structure of FIG. 1 and the description provided by Coyle et al., data from a first device and a second device are not transmitted ***simultaneously over a common bus***. Rather, the system of Coyle et al. transmits data through a plurality of buses where transmission is not simultaneous over a common bus. This claimed feature directed to simultaneous transmission over a common bus is clearly not supported by the structure and description of Coyle et al..

In a similar manner, Coyle et al. further fail to disclose a third device (IOP 2 or MEM 1) transmitting data to the first device (18/20 and SBI 0 or MCU 22) over the bus simultaneously during a second exchange slot. Again, as multiple buses are

used to exchange data by Coyle et al., the combination of claim limitations are clearly not shown in Coyle et al..

On pages 3-4, the Office Action asserts that "[w]ith regards to claims 1-5, one using the device of Coyle et al. would have performed the same steps set forth in claims 1-5" and "[w]ith regards claims 33-38, one using the system of Coyle et al. would have performed the same steps set forth in claims 33-38. See above explanation regarding claims 1-9." These allegations are confusing, at best. On page 3, the Office Action makes reference to claims 1-5 and 1-9, when claims 1, 2, 5, 6 and 9 have been rejected by Coyle et al.. The Office Action asserts that one "would have" performed the same steps. A 102 rejection requires that each and every limitation is shown in a single reference - not whether a limitation "would have" been performed. The Office Action has provided no basis that such steps "would have" been performed by Coyle et al..

Independent claim 39 recites "turn around delay" - which is not addressed by the Office Action in this 102 rejection. As admitted by the Office Action on page 10, Coyle et al. fail to make any mention of "turn around delay." Therefore, this rejection is improper as a 102 rejection where each and every claim limitation must be shown in a single reference because the Office Action admits that a claimed feature is missing from

Coyle et al.. For reasons stated below in connection with claims 3, 4, 7, 8 and 22, an obvious rejection is also improper for lack of sufficient teaching and lack of motivation to modify Coyle et al..

For at least the reasons discussed above, it is respectfully requested that the aforementioned anticipation rejection of claims 1, 2, 5, 6, 9, 17-21, 23 and 33-39 be withdrawn.

B. GARLEEP ET AL. REFERENCE

With respect to the Garleep et al. reference, the Office Action asserts that Garleep et al. teach the present invention as claimed. Applicant respectfully disagrees with the assertions made by the Office Action. In addition, Applicant notes that (1) the present application and Garleep et al. have a common inventor, Frederick A. Ware, and (2) the present application and Garleep et al. are commonly owned. Applicant reserves the right to claim priority to Garleep et al. or to swear behind the filing date of Garleep et al. under a 37 C.F.R. § 1.131 Declaration. Therefore, Applicant submits that upon either action, Garleep et al. is not a proper reference and the rejections of claims 1-14 and 17-39 should be withdrawn.

C. BORKAR ET AL. REFERENCE

With respect to the Borkar et al. reference, the Office Action asserts that Borkar et al. teach the present invention as claimed. However, the Office Action fails to explain how Borkar et al. teach, or even suggest, "a driver configured to provide additive signaling, the driver applying transmit signals to the bus" and "a receiver circuit operably coupled to the driver, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot," as recited in independent claim 10.

Further, the Office Action fails to explain how Borkar et al. teach, or even suggest, "a driver configured to drive a bus with read data during an exchange slot while write data are present on the bus;" "a receiver circuit operably coupled to the driver, the receiver circuit configured to receive the write data from the bus during the exchange slot while the driver is driving the bus with the read data;" and "a memory circuit operably coupled to the receiver circuit, the memory circuit configured to provide the read data and to store the write data," as recited in independent claim 24.

In addition, the Office Action fails to explain how Borkar et al. teach, or even suggest, "a driver configured to drive a

bus with first write data destined for a first memory device during a first exchange slot while first read data from the first memory device are present on the bus" and "a receiver circuit operably coupled to the driver, the receiver circuit configured to receive the first read data from the bus during the first exchange slot while the driver is driving the bus with the first write data," as recited in independent claim 28.

The Office Action addresses the claims (in particular, claims 10, 14 and 15) as containing the phrase "capable of," which according to the Office Action performs a function that is not a positive limitation but only requires the ability to so perform. The Office Action further asserts that it does not constitute a limitation in any patentable sense. Applicant respectfully notes that none of claims 10, 14 or 15 contain that phrase. These claims were previously amended in the Amendment dated October 16, 2003 to recite "a driver configured to provide" in claim 10; "transmit buffers configured to hold data" in claim 14 and "the comparator configured to effectively subtract" in claim 15. In addressing these claims, it is clear that the Office Action has failed to provide proper patentable weight to the recitations. More specifically, the Office Action has improperly construed claims based on terms not recited in the claims. Applicants assert that these claims recite positive

limitations that have not been properly addressed by the Office Action.

With respect to independent claim 10, Borkar et al. fails to show at least a driver configured to provide additive signaling; a receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot.

Claim 12 recites a "terminator operably coupled to the driver and the receiver circuit." However, Borkar et al. specifically teaches that a terminator is not used. "The scheme is self terminating, so that no explicit terminations are required to properly terminate a transmission line" (column 7, lines 29-33).

In addressing independent claims 24 and 28, the Office Action merely states that one using the memory system of Borkar et al. would have performed the same steps set forth in claims 24-32. Applicant respectfully disagrees. Independent claims 24 and 28 recite additional limitations that have not been properly addressed by the Office Action. As the Office Action has failed to meet its burden, the rejections are improper and should be withdrawn.

D. ISHIBASHI ET AL. REFERENCE

With respect to the Ishibashi et al. reference, the Office Action asserts that Ishibashi et al. teach the present invention as claimed. However, the Office Action fails to explain how Ishibashi et al. teach, or even suggest, "a driver configured to provide additive signaling, the driver applying transmit signals to the bus" and "a receiver circuit operably coupled to the driver, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot," as recited in independent claim 10.

Further, the Office Action fails to explain how Ishibashi et al. teach, or even suggest, "a driver configured to drive a bus with read data during an exchange slot while write data are present on the bus;" "a receiver circuit operably coupled to the driver, the receiver circuit configured to receive the write data from the bus during the exchange slot while the driver is driving the bus with the read data;" and "a memory circuit operably coupled to the receiver circuit, the memory circuit configured to provide the read data and to store the write data," as recited in independent claim 24.

In addition, the Office Action fails to explain how Ishibashi et al. teach, or even suggest, "a driver configured to

drive a bus with first write data destined for a first memory device during a first exchange slot while first read data from the first memory device are present on the bus" and "a receiver circuit operably coupled to the driver, the receiver circuit configured to receive the first read data from the bus during the first exchange slot while the driver is driving the bus with the first write data," as recited in independent claim 28.

The Office Action addresses the claims (in particular, claims 10, 14 and 15) as containing the phrase "capable of," which according to the Office Action performs a function that is not a positive limitation but only requires the ability to so perform. The Office Action further asserts that it does not constitute a limitation in any patentable sense. Applicant respectfully notes that none of claims 10, 14 or 15 contain that phrase. These claims were previously amended in the Amendment dated October 16, 2003 to recite "a driver configured to provide" in claim 10; "transmit buffers configured to hold data" in claim 14 and "the comparator configured to effectively subtract" in claim 15. In addressing these claims, it is clear that the Office Action has failed to provide proper patentable weight to the recitations. More specifically, the Office Action has improperly construed claims based on terms not recited in the claims. Applicants assert that these claims recite positive

limitations that have not been properly addressed by the Office Action.

With respect to independent claim 10, Ishibashi et al. fails to show at least a driver configured to provide additive signaling; a receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot.

In addressing independent claims 24 and 28, the Office Action merely states that one using the memory system of Ishibashi et al. would have performed the same steps set forth in claims 24-32. Applicant respectfully disagrees. Independent claims 24 and 28 recite additional limitations that have not been properly addressed by the Office Action. As the Office Action has failed to meet its burden, the rejections are improper and should be withdrawn.

E. DEPENDENT CLAIMS

Claims 2-5 are dependent upon independent claim 1. Thus, since independent claim 1 should be allowable as discussed above, claims 2-5 should also be allowable at least by virtue of their dependency on independent claim 1. Moreover, these claims recite additional features which are not claimed, disclosed, or

even suggested by the cited references taken either alone or in combination.

Claims 7-9 are dependent upon independent claim 6. Thus, since independent claim 6 should be allowable as discussed above, claims 7-9 should also be allowable at least by virtue of their dependency on independent claim 6. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

Claims 11-16 are dependent upon independent claim 10. Thus, since independent claim 10 should be allowable as discussed above, claims 11-16 should also be allowable at least by virtue of their dependency on independent claim 10. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

Claims 18-23 are dependent upon independent claim 17. Thus, since independent claim 17 should be allowable as discussed above, claims 18-23 should also be allowable at least by virtue of their dependency on independent claim 17. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

Claims 25-27 are dependent upon independent claim 24. Thus, since independent claim 24 should be allowable as discussed above, claims 25-27 should also be allowable at least by virtue of their dependency on independent claim 24. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

Claims 29-32 are dependent upon independent claim 28. Thus, since independent claim 28 should be allowable as discussed above, claims 29-32 should also be allowable at least by virtue of their dependency on independent claim 28. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

Claims 34-38 are dependent upon independent claim 33. Thus, since independent claim 33 should be allowable as discussed above, claims 34-38 should also be allowable at least by virtue of their dependency on independent claim 33. Moreover, these claims recite additional features which are not claimed, disclosed, or even suggested by the cited references taken either alone or in combination.

In view of the foregoing, it is respectfully requested that the aforementioned anticipation rejection of claims 1-14, 16-39 be withdrawn.

III. THE OBVIOUSNESS REJECTION OF CLAIMS 3, 4, 7, 8, 15, 16 and 22

On page 10 of the Office Action, claims 3, 4, 7, 8 and 22 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Coyle et al.. On page 11 of the Office Action, claims 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Garleep et al.. These rejections are hereby respectfully traversed.

Under 35 U.S.C. § 103, the Patent Office bears the burden of establishing a prima facie case of obviousness. As stated in MPEP § 2143, to establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the

reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.

A. COYLE ET AL. - 103 REJECTION

The Office Action asserts that it would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide Coyle et al. with "turn around delay" between time slows, since the Examiner takes Official Notice that using a turn around delay between time slots are old and well known for preventing data interference; and using such a "turn around delay" in Coyle et al. involves only routine skill in the art.

The Examiner alleges that "turn around delay" between time slots are old and well known. The Applicant traverses this rejection because there is no support in the record for the conclusion that the identified features are "old and well known." In accordance with MPEP § 2144.03, the Examiner must cite a reference in support of his position.

For a proper 103 rejection, there must be some motivation to modify the primary reference as suggested by the Office Action. Any such motivation is completely lacking. The Office Action states that a turn around delay between time slots are old and well known for preventing data interference. However, this is not a perceived problem in the Coyle et al. reference.

What is fundamentally lacking in this analysis is any indication in any of the art that data interference is a problem that needs to be solved by turn around delay. The Office Action's statement of motivation is a clear example of improper hindsight.

Controlling Federal Circuit and Board precedent require that the Office Action set forth specific and particularized motivation for one of ordinary skill in the art to modify a primary reference to achieve a claimed invention. *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 664 (Fed. Cir. 2000) ("[t]o prevent a hindsight-based obviousness analysis, [the Federal Circuit has] clearly established that the relevant inquiry for determining the scope and content of the prior art is whether there is a reason, suggestion, or motivation in the prior art or elsewhere that would have led one of ordinary skill in the art to combine the references.").

Here, there has been no citation of any teaching anywhere in the art of any need for a implementing turn around delay. The Office Action has failed to identify any teaching of that problem specifically. When a primary reference is missing elements, the law of obviousness requires that the Office Action set forth some motivation why one of ordinary skill in the art would have been motivated to modify the primary reference in the exact manner proposed. *Ruiz*, 234 F.3d at 664. In other words, there must be some recognition that the primary reference has a problem and that the proposed modification will solve that exact problem. All of this motivation must come from the teachings of the prior

art to avoid impermissible hindsight looking back at the time of the invention. Because such a proper motivation to combine is missing, the combinations are improper and the rejections should be overturned.

If the approach taken by this Office Action were adopted, in almost every instance, some reason for a modifying a reference could be impermissibly created, unrelated to any actual problem recognized in the art. It is the requirement that the motivation to solve a recognized problem be from the teachings of the art that keeps the application process honest to the goal of avoiding hindsight reconstruction. Indeed, the very key aspect in determining obviousness should be that there is a clear nexus between the teachings in the art as to the deficiencies in a particular way of doing things and a solution provided by the supplemental references.

The absence of a teaching is the fundamental problem with the rejections proposed by the Office Action and the reason why these combinations are improper. Therefore, there must be some motivation to combine the elements besides for the sake of combining the references. In addition, even if the references could be combined as proposed, the resulting combination would nevertheless fail to render the claim inventions obvious.

Therefore, it is respectfully submitted that the rejections of claims 3, 4, 7, 8 and 22 should be withdrawn and the claims allowed accordingly.

B. GARLEEP ET AL. - 103 REJECTION

On page 11 of the Office Action, claims 15 and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Garleep et al..

COMMON OWNERSHIP under 35 U.S.C. § 103(c)

35 U.S.C. § 103(c) states the following:

> Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

The application and the Garleep et al. patent were, at the time the invention was made, owned by Rambus Inc.

As commonly ownership has been established, Garleep et al. is not valid prior art under 35 U.S.C. § 103(c).

In view of the foregoing, it is respectfully requested that the aforementioned obviousness rejection of claims 3, 4, 7, 8, 15, 16 and 22 be withdrawn.

It is further believed that the rejections directed to claims 1-39 are improper and should be withdrawn.

IV. CONCLUSION

In view of the foregoing, it is respectfully submitted that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number, in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

To the extent necessary, a petition for an extension of time under 37 CFR § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-0206, and please credit any excess fees to the same deposit account.

Respectfully submitted,
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APPENDIX A

Fig. 4 is a block diagram illustrating one embodiment of a pair of devices coupled by a conductor in accordance with an embodiment of the invention. Device 401 is coupled to device 402 via conductor 403. Devices 401 and 402 may be any of several devices coupled to a bus comprising conductor 403. Different pairs of devices may be scheduled to communicate with each other during different exchange slots on the bus. In this embodiment, neither device 401 nor device 402 has a transmit buffer. Rather, the scheduling of exchange slots takes into account the times at which the devices will have information to communicate with each other and schedules exchange slots to utilize conductor 403 accordingly. During the exchange slot, device 401 transmits information over conductor 403 to device 402 via 404, while, at the same time, device 402 transmits information over conductor 403 to device 401 via 405.

APPENDIX B

Thus, information to be written to a memory device implemented as device 502 may be held in transmit buffer 506 of a memory controller implemented as device 501 until information is desired to be read from device 502. When information is desired to be read from device 502, an exchange slot is scheduled for communication along a bus comprising conductor 503 between device 501 and device 502. During the exchange slot, the desired information is read from device 502 and transmitted to device 501 via 505, and, at the same time, information being held in transmit buffer 506 is transmitted to device 502 via 504.

APPENDIX C

When an amount of information to be transmitted is received in either transmit buffer 606 or transmit buffer 607 such that any specified criteria for requesting an exchange slot are met, an exchange slot is requested. A scheduler, which may, for example, be a common scheduler or cooperative schedulers, allocates an exchange slot for devices 601 and 602 to use a bus comprising conductor 603. During the exchange slot, device 601 transmits the information from transmit buffer 606 destined for device 602 to device 602 over conductor 603 When an amount of information to be transmitted is received in either transmit buffer 606 or transmit buffer 607 such that any specified criteria for requesting an exchange slot are met, an exchange slot is requested. A scheduler, which may, for example, be a common scheduler or cooperative schedulers, allocates an exchange slot for devices 601 and 602 to use a bus comprising conductor 603. During the exchange slot, device 601 transmits the information from transmit buffer 606 destined for device 602 to device 602 over conductor 603. At the same time, device 602 transmits the information from transmit buffer 607 destined for device 601 to device 601 over conductor 603 via 604. At the same time, device 602 transmits the information from transmit buffer 607 destined for device 601 to device 601 over conductor 603 via 605.

APPENDIX D

Fig. 7 is a block diagram illustrating a pair of devices coupled by a conductor in accordance with an embodiment of the invention. Device 701 is coupled to device 702 via conductor 703. Devices 701 and 702 may be any of several devices coupled to a bus comprising conductor 703. Different pairs of devices may be scheduled to communicate with each other during different exchange slots on the bus. In this embodiment, device 701 includes transmit buffer 706 and receive buffer 708, and device 702 includes transmit buffer 707 and receive buffer 709. While the transmit buffers may be used as described in reference to Fig. 6, the receive buffers may be used to receive information transmitted over conductor 703 via 704 and 705, until other circuits within devices 701 and 702 are ready to process the received information. While receive buffers are illustrated in Fig. 7, it should be understood that any of the configurations illustrated in Figs. 4, 5, and 6 may be implemented with receive buffers in either or both of the devices coupled to the conductor.

APPENDIX E

1 (Original). A method for providing simultaneous bidirectional signaling in a bus topology comprising the steps of:

selecting a first device and a second device from among a plurality of devices operably coupled to a common bus to exchange a first set of data;

scheduling a first exchange slot over which the first device and the second device are to exchange the first set of data; and

during the first exchange slot, simultaneously transmitting a first portion of the first set of data from the first device to the second device over the common bus and transmitting a second portion of the first set of the data from the second device to the first device over the common bus.

2 (Original). The method of claim 1 further comprising the steps of:

selecting the first device and a third device to exchange a second set of data;

scheduling a second exchange slot over which the first device and the third device are to exchange the second set of data; and

during the second exchange slot, simultaneously

transmitting a first portion of the second set of data from the first device to the third device over the common bus and transmitting a second portion of the second set of the data from the third device to the first device over the common bus.

3 (Original). The method of claim 2 further comprising the step of:

introducing a turnaround delay between the first exchange slot and the second exchange slot.

4 (Original). The method of claim 3 wherein the turnaround delay is less than twice an end-to-end propagation delay of the common bus.

5 (Original). The method of claim 1 wherein the first device is a memory controller, and the second device is a memory device and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

6 (Previously Presented). A system providing simultaneous bidirectional signaling using a bus topology, the system

comprising:

a first device operably coupled to a bus;

a second device operably coupled to the bus, the first device transmitting a first portion of a first set of data over the bus to the second device and the second device transmitting a second portion of the first set of data over the bus to the first device simultaneously during a first exchange slot; and

a third device operably coupled to the bus, the first device transmitting a first portion of a second set of data over the bus to the third device and the third device transmitting a second portion of the second set of data over the bus to the first device simultaneously during a second exchange slot.

7 (Original). The system of claim 6 wherein a turnaround delay exists between the first exchange slot and the second exchange slot.

8 (Original). The system of claim 7 wherein the turnaround delay is less than twice an end-to-end propagation delay of the bus.

9 (Original). The system of claim 6 wherein the first device is a memory controller, and the second device is a memory device

and wherein the first portion of the first set of data and the first portion of the second set of data are write data and the second portion of the first set of data and the second portion of the second set of data are read data.

10 (Previously Presented). A device coupled to a bus in a bus topology for providing simultaneous bidirectional signaling, the device comprising:

a driver configured to provide additive signaling, the driver applying transmit signals to the bus;

a receiver circuit operably coupled to the driver, the receiver circuit configured to effectively subtract the transmit signals to receive received signals from the bus, the driver and the receiver circuit operating during an exchange slot.

11 (Original). The device of claim 10 wherein the device is coupled to the bus by an impedance-matching splitter.

12 (Original). The device of claim 10 wherein the device further comprises:

a terminator operably coupled to the driver and the receiver circuit, the terminator providing a controlled termination impedance.

13 (Original). The device of claim 10 wherein the device further comprises:

a transmit circuit operably coupled to the driver, the transmit circuit comprising a transmit buffer, the transmit buffer holding data pending arrival of the exchange slot.

14 (Previously Presented). The device of claim 13 wherein the transmit buffer further comprises:

a plurality of transmit buffers, the plurality of transmit buffers configured to hold data destined for different other devices.

15 (Previously Presented). The device of claim 13 wherein the receiver circuit further comprises:

a comparator operably coupled to the transmitter and to the driver, the comparator configured to effectively subtract the transmit signals to yield received signals from the bus; and

a receiver operably coupled to the comparator, the receiver receiving the received signals and obtaining received data from the received signals.

16 (Previously Presented). The device of claim 15 further

comprising:

an enabling circuit, coupled to the transmit circuit and the receive circuit, responsive to an exchange slot indication, the enabling circuit enabling the operation of the transmit circuit and the receive circuit during the exchange slot.

17 (Previously Presented). A memory system comprising:

a memory controller;

a bus operably coupled to the memory controller;

a first memory device operably coupled to the bus, the first memory device configured to simultaneously send first read data to the memory controller via the bus and receive first write data from the memory controller via the bus; and

a second memory device operably coupled to the bus, the second memory device configured to simultaneously send second read data to the memory controller via the bus and receive second write data from the memory controller via the bus.

18 (Previously Presented). The memory system of claim 17 wherein the first memory device is configured to simultaneously send the first read data to the memory controller and receive the first write data from the memory controller during a first exchange slot and wherein the second memory device is configured

to simultaneously send the second read data to the memory controller and receive the second write data from the memory controller during a second exchange slot.

19 (Original). The memory system of claim 18 wherein the memory controller comprises:

a first write buffer to hold the first write data pending arrival of the first exchange slot.

20 (Original). The memory system of claim 19 wherein the memory controller comprises:

a second write buffer to hold the second write data pending arrival of the second exchange slot.

21 (Previously Presented). The memory system of claim 17 wherein the bus comprises:

a conductor operably coupling the first memory device and the second memory device to the memory controller, wherein the first memory device is configured to simultaneously send a first read bit of the first read data to the memory controller over the conductor and receive a first write bit of the first write data from the memory controller over the conductor during a first exchange slot and wherein the second memory device is

configured to simultaneously send a second read bit of the second read data to the memory controller over the conductor and receive a second write bit of the second write data from the memory controller over the conductor during a second exchange slot.

22 (Original). The memory system of claim 21 wherein a turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

23 (Original). The memory system of claim 17 wherein the memory controller performs coherency checking during memory access operations.

24 (Previously Presented). A memory device comprising:

a driver configured to drive a bus with read data during an exchange slot while write data are present on the bus;

a receiver circuit operably coupled to the driver, the receiver circuit configured to receive the write data from the bus during the exchange slot while the driver is driving the bus with the read data; and

a memory circuit operably coupled to the receiver circuit,

the memory circuit configured to provide the read data and to store the write data.

25 (Previously Presented). The memory device of claim 24 further comprising:

an enabling circuit responsive to an exchange slot indication, the enabling circuit operably coupled to the driver and the receiver circuit, the enabling circuit enabling interaction of the driver and the receiver circuit with the bus during the exchange slot.

26 (Previously Presented). The memory device of claim 25 wherein the enabling circuit is configured to be responsive to the exchange slot indication following a turnaround delay sufficient to prevent inter-symbol interference.

27 (Original). The memory device of claim 24 further comprising:

a transmit circuit operably coupled to the driver, the transmit circuit comprising a transmit buffer, the transmit buffer holding the read data pending arrival of the exchange slot.

28 (Previously Presented). A memory controller comprising:

a driver configured to drive a bus with first write data destined for a first memory device during a first exchange slot while first read data from the first memory device are present on the bus;

a receiver circuit operably coupled to the driver, the receiver circuit configured to receive the first read data from the bus during the first exchange slot while the driver is driving the bus with the first write data.

29 (Previously Presented). The memory controller of claim 28 wherein the driver is further configured to drive the bus with second write data destined for a second memory drive during a second exchange slot while second read data from the second memory device are present on the bus and wherein the receiver circuit is further configured to receive the second read data from the bus during the second exchange slot while the driver is driving the bus with the second write data.

30 (Original). The memory controller of claim 29 wherein a turnaround delay sufficient to prevent inter-symbol interference is introduced between the first exchange slot and the second exchange slot.

31 (Original). The memory controller of claim 28 further comprising:

a transmit circuit operably coupled to the driver to transmit the first write data and the second write data to the driver, the transmit circuit comprising a transmit buffer to hold the first write data pending arrival of the first exchange slot and the second write data pending arrival of the second exchange slot.

32 (Original). The memory controller of claim 31 wherein the transmit buffer comprises:

a first transmit buffer to hold the first write data pending arrival of the first exchange slot; and

a second memory buffer to hold the second write data pending arrival of the second exchange slot.

33 (Original). A method for providing simultaneous bidirectional communication between a memory controller and a plurality of memory devices comprising the steps of:

during a first exchange slot, simultaneously communicating over a common bus first write data from the memory controller to a first memory device of the plurality of memory devices and first read data from the first memory device to the memory

controller; and

during a second exchange slot, simultaneously communicating over a common bus second write data from the memory controller to a second memory device of the plurality of memory devices and second read data from the second memory device to the memory controller.

34 (Original). The method of claim 33 further comprising the step of:

holding the first write data destined for the first memory device in the memory controller pending arrival of the first exchange slot.

35 (Original). The method of claim 34 further comprising the step of:

holding the second write data destined for the second memory device in the memory controller pending arrival of the second exchange slot.

36 (Original). The method of claim 35 wherein the step of holding the first write data occurs in a first write buffer and wherein the step of holding the second write data occurs in a second write buffer.

37 (Original). The method of claim 35 further comprising the steps of:

holding the first read data destined for the memory controller in the first memory device; and

holding the second read data destined for the memory controller in the second memory device.

38 (Original). The method of claim 37 wherein the step of simultaneously communicating over the common bus the first write data from the memory controller to the first memory device and the first read data from the first memory device to the memory controller occurs after a specified amount of the first write data destined for the first memory device is hold in the memory controller.

39 (Previously Presented). A system for bidirectional communication of data over a common bus comprising:

a first device operably coupled to the common bus, the first device comprising a first-to-second transmit buffer to hold first-to-second data and a first-to-third transmit buffer to hold first-to-third data;

a second device operably coupled to the common bus, the

second device comprising a second-to-first transmit buffer to hold second-to-first data;

a third device operably coupled to the common bus, the third device comprising a third-to-first transmit buffer to hold third-to-first data; and

a scheduler operably coupled to the common bus, the scheduler scheduling the first device to transmit the first-to-second data and the second device to transmit the second-to-first data over the common bus simultaneously during a first exchange slot and scheduling the first device to transmit the first-to-third data and the third device to transmit the third-to-first data over the common bus simultaneously during a second exchange slot, the scheduler introducing a turnaround delay sufficient to prevent inter-symbol interferences between the first exchange slot and the second exchange slot.